CLAIMS

What is claimed is:

1. A processor comprising:

a microcode sequencer to set an identifier in a microinstruction, the identifier indicating one of a plurality of copies of broadcast state of the processor; and

a functional unit to receive and internally store the plurality of copies of broadcast state and to select, based on the identifier, one of the copies of broadcast state for use in processing the microinstruction.

2. A processor as recited in claim 1, further comprising a memory execution unit including a segment register, said broadcast state representing content of the segment register.

3. A processor as recited in claim 2, further comprising a renamer to selectively rename registers of the processor, including the segment register, wherein each of the copies of broadcast state may correspond to a different renamed version of the segment register.

4. A processor as recited in claim 1, further comprising a trace cache to maintain the identifier for at least some of the microinstructions.

5. A processor as recited in claim 1, wherein the microcode sequencer comprises a broadcast state machine to determine the identifier.

6. A processor as recited in claim 1, further comprising a second functional unit to receive and internally store a second plurality of different copies of broadcast state of the processor and to select, based on the identifier in a microinstruction, one of the second plurality of copies of broadcast state for use in processing the microinstruction.

7. A processor comprising:

means for generating an identifier field in a microinstruction, the identifier field indicating one of a plurality of copies of broadcast state of the processor to be used in processing a microinstruction; and

a functional unit including

means for receiving and internally storing the plurality of copies of broadcast state, and

means for selecting one of the copies of broadcast state indicated by the identifier field, and

means for processing the microinstruction using the selected copy of broadcast state.

8. A processor as recited in claim 7, further comprising a memory execution unit including a segment register, said broadcast state representing content of the segment register.

9. A processor as recited in claim 8, wherein each of the copies of broadcast state may correspond to a different renamed version of the segment register.

10. A processor as recited in claim 7, further comprising a trace cache to maintain the identifier field for at least some of the microinstructions.

11. A processor comprising:

a memory execution unit including a segment register, content of the segment register representing state of the processor;

a microcode sequencer to sequence microinstructions for execution in the processor, including setting an identifier field in at least some of the microinstructions, the identifier field of each such microinstruction indicating one of a plurality of copies of broadcast state of the processor to be used in processing the microinstruction; and

a functional unit to receive and internally store the plurality of copies of broadcast state and to select, based on the identifier field of a microinstruction, one of the copies for use in processing the microinstruction.

12. A processor as recited in claim 11, further comprising a renamer to selectively rename registers of the processor, including the segment register, wherein each of the copies of broadcast state may correspond to a different renamed version of the segment register.

13. A processor as recited in claim 11, further comprising a trace cache to maintain the identifier field for at least some of the microinstructions.

14. A processor as recited in claim 11, wherein the microcode sequencer comprises a broadcast state machine to determine the identifier field.

15. A processor as recited in claim 11, further comprising a second functional unit to receive and internally store a second plurality of different copies of broadcast state of the processor and to select, based on the identifier field of a microinstruction, one of the second plurality of copies for use in processing the microinstruction.

16. A microprocessor comprising:

a memory execution unit including a segment register file containing a segment register, content of the segment register representing state of the microprocessor to be broadcast within the microprocessor;

a renamer to selectively rename registers of the processor, including the segment register;

a microcode sequencer to sequence microinstructions for execution in the processor, including setting an identifier field in at least some of the microinstructions, the identifier field of each such microinstruction indicating one of a plurality of different copies of broadcast state of the microprocessor to be used

in processing the microinstruction, each copy of broadcast state corresponding to a different renamed version of the segment register; and

a functional unit to receive and internally store the plurality of different copies of broadcast state and to select, based on the identifier field of a microinstruction, one of the copies for use in processing the microinstruction.

17. A processor as recited in claim 16, further comprising a trace cache to maintain the identifier field for at least some of the microinstructions.

18. A processor as recited in claim 16, wherein the microcode sequencer comprises a broadcast state machine to determine the identifier field.

19. A processor as recited in claim 16, further comprising a second functional unit to receive and internally store a second plurality of different copies of broadcast state of the microprocessor and to select, based on the identifier field of a microinstruction, one of the second plurality of copies for use in processing the microinstruction.

20. A method comprising:

storing a plurality of copies of broadcast state of a processor in each of a plurality of functional units of the processor;

issuing a microinstruction in the processor, the microinstruction including an identifier; and

using the identifier in at least one of the functional units to select one of the plurality of copies of broadcast state for use in processing the microinstruction.

21. A method as recited in claim 20, wherein said broadcast state represents content of a segment register of the processor.

22. A method as recited in claim 21, wherein each of the copies of broadcast state may correspond to a different renamed version of the segment register.

23. A method as recited in claim 20, further comprising using a microcode sequencer of the processor to provide the identifier.

24. A method as recited in claim 20, further comprising using a trace cache of the processor to provide the identifier.

25. A method comprising:

providing an identifier field in a microinstruction for execution in a processor, the identifier field indicating one of a plurality of copies of broadcast state of the processor to be used in processing the microinstruction;

storing the plurality of copies of broadcast state in a functional unit of the processor, and

selecting one of the copies of broadcast state in the functional unit, for use in processing the microinstruction, according to the identifier field of the microinstruction.

26. A method as recited in claim 25, further comprising storing a plurality of copies of broadcast state in each of a plurality of functional units of the processor.

27. A method as recited in claim 25, wherein said broadcast state represents content of a segment register of the processor.

28. A method as recited in claim 27, wherein each of the copies of broadcast state may correspond to a different renamed version of the segment register.

29. A method as recited in claim 25, further comprising using a microcode sequencer of the processor to provide the identifier field.

30. A method as recited in claim 25, further comprising using a trace cache of the processor to provide the identifier field.